Amendments to the Claims:

This listing of claims replaces all prior versions, and listings, of claims in the application.

Listing of claims:

1. (Currently Amended) A semiconductor integrated circuit comprising:

a plurality of data input pins for receiving data signals in a normal mode and at least one of the plurality of data input pins for receiving test signals in a test mode, such that the data input pins can receive both the data signals and the test signals;

a plurality of data output pins;

a test pin;

a data processing circuit for generating output signals in response to input signals; and

an output circuit for outputting the output signals to the data output pins in [[a]]the normal mode and sequentially outputting the output signals to the test pin in response to a clock signal in [[a]]the test mode.

2. (Original) The integrated circuit of claim 1, wherein the output circuit controls the output signals not to be outputted to the data output pins in the test mode.

3. (Withdrawn) A semiconductor integrated circuit comprising:

a plurality of output pins;

a test pin;

a data processing circuit for generating output signals in response to input signals and transferring the generated output signals to the data output pins, and

an output circuit for sequentially outputting the output signals to the test pin in response to a clock signal.

4. (Withdrawn) The integrated circuit of claim 3, wherein the output circuit comprises a shift register operating in response to the clock signal.

5. (Currently Amended) A method for receiving test data signals and outputting data in a test mode of a semiconductor integrated circuit with a plurality of data input pins and a plurality of data output pins and a test pin, comprising:

receiving data signals at the plurality of data input pins during a normal mode and receiving test data signals at the plurality of data input pins during the test mode, such that the data input pins can receive both the data signals and the test signals;

determining whether the test mode is activated; and

sequentially outputting the output signals to the test pin in response to a clock signal in the test mode.

6. (Original) The method of claim 5, further comprising outputting the output signals to the data output pins if the test mode is not activated.